

# Introduction to Artifact Evaluation

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# What is an Artifact?

An artifact is a supplement that extends beyond a scientific paper and supports the claims or results of that paper.

Artifact may contain: software, mechanized proofs, test suites, data sets, benchmarks, video of a difficult/impossible-to-share system in use, hardware, or any other artifact described in a paper.

An artifact captures a point-in-time matching the paper. It should be packaged for long-term preservation to facilitate future research.

# Artifact Evaluation Motivations

- Encourage and support authors to provide supplements to papers
- Help future researchers to more effectively build on and compare with previous work
- Validate claims and results presented in a paper
- Reward authors who put in effort to create useful artifacts
- Recognize the effort to release usable software systems

# Papers with artifacts are recognized with badges.

**KFormat2: an SMT-Based Model Checker for Imperative Programs\***



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**Abstract.** This work introduces KFormat2, which is the evolution of the model checker KFormat from a domain-specific tool for verifying the correctness of dataflow analysis algorithms to a general-purpose tool for verifying the correctness of imperative programs. It is implemented in the SMT solver CVC5 and supports a rich set of user-defined predicates for expressing domain-specific properties. KFormat2 is a first step towards a general-purpose model checker for imperative programs, which can be used to verify the correctness of domain-specific algorithms and dataflow analysis algorithms. It is implemented in the SMT solver CVC5 and supports a rich set of user-defined predicates for expressing domain-specific properties.

**1 INTRODUCTION**

We present KFormat2, which is the evolution of the model checker KFormat from a domain-specific tool for verifying the correctness of dataflow analysis algorithms to a general-purpose tool for verifying the correctness of imperative programs. It is implemented in the SMT solver CVC5 and supports a rich set of user-defined predicates for expressing domain-specific properties. KFormat2 is a first step towards a general-purpose model checker for imperative programs, which can be used to verify the correctness of domain-specific algorithms and dataflow analysis algorithms. It is implemented in the SMT solver CVC5 and supports a rich set of user-defined predicates for expressing domain-specific properties.



**Merchandise: Data Placement on Heterogeneous Memory for Task-Parallel HPC Applications with Load-Balance Awareness**

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**Abstract.** The emergence of heterogeneous memory (HMM) provides a novel effective and high-performance solution to memory-constrained HPC applications. Designing the placement of data objects on HMM is critical for high performance. This work is a performance-oriented and data placement on HMM for task-parallel HPC applications. The rest of the problem is that being composed of parallel task execution and an invariant assumption that being frequently accessed pages to find memory after task to better performance. In addition, this problem, we introduce a load-balance-aware page management scheme. Instead of traditional first-come-first-served task scheduling, design memory profiling, reduce task being application-specific. Using the heuristic task scheduling, Merchandise effectively sets up execution time among tasks in the range of 50% to 60% of tasks that are not of only considering any individual task. Meanwhile, this is highly consistent with high stability. Evaluating with memory-constrained HPC applications, we show that Merchandise reduces load imbalance and task-to-task average of 37.5% and 64.1% (up to 26% and 23.2%) performance over traditional first-come-first-served task scheduling and an industry quality software-based solution.

**CCS Concepts:** Computer systems organization — Heterogeneous (hybrid) systems; Theory of computation — Parallel computing models; Hardware — Non-volatile memory

**Keywords:** Data Placement; Heterogeneous Memory; Parallel Computing; Load Balance

**ACM Reference Format:** Xie, Zhen, Liu, Jin, and Li, Yang. Merchandise: Data Placement on Heterogeneous Memory for Task-Parallel HPC Applications with Load-Balance Awareness. In *Proceedings of the ACM Symposium on Principles and Practice of Parallel Programming (PPoPP '22)*. Artur M. M. Correia, Ed. ACM, 2022, 6 pages. <https://doi.org/10.1145/3529366.3529367>

**1 INTRODUCTION**

Many high-performance computing (HPC) applications are becoming increasingly dependent on heterogeneous memory, which is a natural extension of memory. This work is a performance-oriented and data placement on HMM for task-parallel HPC applications. The rest of the problem is that being composed of parallel task execution and an invariant assumption that being frequently accessed pages to find memory after task to better performance. In addition, this problem, we introduce a load-balance-aware page management scheme. Instead of traditional first-come-first-served task scheduling, design memory profiling, reduce task being application-specific. Using the heuristic task scheduling, Merchandise effectively sets up execution time among tasks in the range of 50% to 60% of tasks that are not of only considering any individual task. Meanwhile, this is highly consistent with high stability. Evaluating with memory-constrained HPC applications, we show that Merchandise reduces load imbalance and task-to-task average of 37.5% and 64.1% (up to 26% and 23.2%) performance over traditional first-come-first-served task scheduling and an industry quality software-based solution.

**ARTICLE HISTORY:** Received 12 October 2021; revised 16 February 2022; accepted 22 February 2022. Published by ACM on 01 July 2022.

**A Retrospective Study of One Decade of Artifact Evaluations**

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**ABSTRACT.** This paper reporting research involves the development of a prototype of artifact evaluation as a measurement system. It differs with the others conducted in the research process, they are software-oriented to search artifacts and compare with software evaluation. In a specific evaluation, this is compared with the software engineering research in IEEE, ACM, both the work and the process. It has been adopted and other experiments. This work is a retrospective study of one decade of artifact evaluations. This paper reports the results and compares with the work on artifact evaluation. This work is a retrospective study of one decade of artifact evaluations. This paper reports the results and compares with the work on artifact evaluation. This work is a retrospective study of one decade of artifact evaluations. This paper reports the results and compares with the work on artifact evaluation.

**KEYWORDS:** Artifact evaluation, artifact evaluation system, open-source development, reuse, long-term reliability of software and data, artifact evaluation system

**1 INTRODUCTION**

The emergence of HPC applications has led to the development of HMM. This work is a performance-oriented and data placement on HMM for task-parallel HPC applications. The rest of the problem is that being composed of parallel task execution and an invariant assumption that being frequently accessed pages to find memory after task to better performance. In addition, this problem, we introduce a load-balance-aware page management scheme. Instead of traditional first-come-first-served task scheduling, design memory profiling, reduce task being application-specific. Using the heuristic task scheduling, Merchandise effectively sets up execution time among tasks in the range of 50% to 60% of tasks that are not of only considering any individual task. Meanwhile, this is highly consistent with high stability. Evaluating with memory-constrained HPC applications, we show that Merchandise reduces load imbalance and task-to-task average of 37.5% and 64.1% (up to 26% and 23.2%) performance over traditional first-come-first-served task scheduling and an industry quality software-based solution.

# Historical Background

Insufficient respect paid to the artifacts that back papers.

Areas so centered on software, models, and specifications should want to evaluate artifacts as part of the paper review process.

Not examining artifacts enables everything from mere sloppiness to, in extreme cases, dishonesty.

More subtly, it also imposes a subtle penalty on people who take the trouble to vigorously implement and test their ideas.

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Source: [artifact-eval.org/motivation](http://artifact-eval.org/motivation)

*In 2011, Andreas Zeller, the program chair for ESEC/FSE, decided to institute a committee to address this problem. Andreas asked Carlo Ghezzi and Shriram Krishnamurthi to run this process.*

*Shriram had long wanted to create such a committee and call it the "Program Committee" (ha, ha). However, not only is that name taken, we also wanted to be open-minded to all sorts of artifacts that are not programs [...]. We therefore called this the **Artifact Evaluation Committee (AEC)**.*

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Source: [artifact-eval.org/motivation](http://artifact-eval.org/motivation)

## **Software Engineering & Programming Languages conferences**

ICSE, ESEC/FSE, ASE, ECOOP, ISSTA, OOPSLA, POPL, PLDI, ICFP, SAS, ESOP, TACAS, CAV...

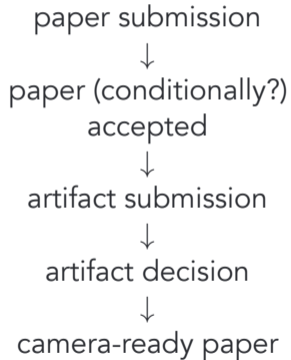
## **Top SE/PL journals**

TSE, TOSEM, EMSE, TOPLAS...

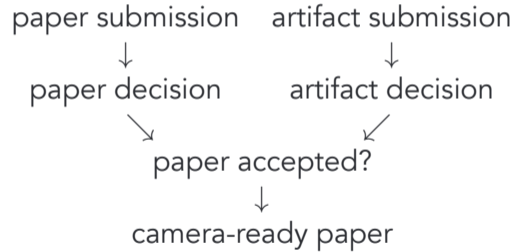
## **Systems research**

SOSP, USENIX ATC, EuroSys, FAST, OSDI, SC...

## Common



## Alternative





# Artifact Evaluation Process

| Time      | Step                             | Responsible party |
|-----------|----------------------------------|-------------------|
|           | Artifact submission              | Authors           |
| 2–5 days  | Bidding                          | AEC members       |
|           | Artifacts assigned (usually 2–3) | AEC chairs        |
| 1–2 weeks | <b>Phase 1:</b> Kick the tires   | AEC members       |
| 1–2 weeks | Author responses, possible fixes | Authors           |
| 2–4 weeks | <b>Phase 2:</b> Full review      | AEC members       |
| 3–7 days  | Discussion and badging decisions | AEC members       |
|           | Decisions announced              | AEC chairs        |

Expect an artifact to take on average 8h to review completely.

Artifacts are evaluated against badging criteria. The current commonly applied criteria is ACM Artifact Review and Badging policy v1.1.



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<https://www.acm.org/publications/policies/artifact-review-and-badging-current>



Author-created artifacts relevant to the paper have been placed on a publicly accessible *archival repository*.

A DOI or link to this repository along with a unique identifier for the object is provided.

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Archival repositories: Zenodo, Figshare, Software Heritage, Dagstuhl Artifacts Series (DARTS),...

# Badges: Artifacts Evaluated



**Functional** The artifacts associated with the research are found to be *documented, consistent, complete, exercisable*, and include appropriate evidence of verification and validation.



**Reusable** The artifacts have all the qualities of Functional level, but, in addition, they are very carefully documented and well-structured to the extent that reuse and repurposing is facilitated.

# Badges: Results Validated



**Reproduced** The main results of the paper have been obtained in a subsequent study by a person or team other than the authors, *using, in part, artifacts provided by the author.*



**Replicated** The main results of the paper have been independently obtained in a subsequent study by a person or team other than the authors, *without the use of author-supplied artifacts.*

AEC members are usually senior graduate students, postdocs, or recent PhD graduates.

Among researchers, experienced graduate students are often in the best position to handle the diversity of systems expectations that the AEC will encounter.

Graduate students represent the future of the community, so involving them in the AEC process early will help push this process forward.

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Source: <https://pldi24.sigplan.org/track/pldi-2024-pldi-research-artifacts>

# Benefits of Participating in AECs

- Early experience in peer review process, learn how to write reviews
- Early access to cutting-edge works at top conferences
- Gain exposure to new research topics
- Develop intuition for what a top-conference publication requires
- Learn the artifact process and improve quality of own artifacts
- Start recognizing researchers, research trends, etc.
- Service experience for your CV

# General Artifact Preparation Tips

- Make artifact claims explicit in the artifact readme
- Prepare a push-button/single command evaluation
- If paper has tables and figures of measurements, the artifact should support re-generating these
- Remember a license



# General Artifact Preparation Tips

For long evaluations:

- Prepare a small evaluation ( $\sim 10$  min) + full evaluation
- Try include difficult cases in the small evaluation
- Provide time estimates of all long latency tasks

Artifact should be useful long-term ( $\geq 10$  years)

- Provide a container or VM that captures the expected environment
- Detail software dependencies, including versions
- Make artifact self-contained: avoid external references that may change or get deleted